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The *BELLPAC** Modular Electronic Packaging System

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The BELLPAC* *system is a family of electronic packaging modules being used in the physical design of more than 40 new Bell Laboratories-developed systems. The* BELLPAC *system consists of a set of circuit packs, connectors (both circuit pack and backplane), and shelf hardware. A range of circuit pack sizes and interconnection densities is provided to match system packaging needs. Present elements include circuit pack connectors with pin-outs ranging from 50 to 300, circuit pack sizes ranging from 30 to 100 square inches, and circuit pack technologies ranging from simple, low-density, epoxy glass (or epoxy-coated metal) circuits up to fine-line multilayer boards. In this paper, we review the physical design of the* BELLPAC *system. We also describe the large body of design and manufacturing support information available to system development organizations using* BELLPAC *hardware.*

I. HISTORY AND DEVELOPMENT GOALS

The *BELLPAC** system, formerly known as CDCP (Common Design Circuit Packaging), grew out of a working committee established in 1975 and led by J. G. Brinsfield of the Interconnection Technology Laboratory at Bell Laboratories in Whippany, New Jersey. Committee representatives from each system development area, from Western Electric, and from the electronic components area established the following goal for their work:

> By the use of standard physical design, to reduce the costs and time intervals required to develop and manufacture new systems.

The committee also established requirements that were felt neces-

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sary for the wide acceptance of a standardized set of hardware building blocks. Among these were the following objectives:

(*i*) Design packaging modules to provide the correct trade-offs between flexibility and cost.

(*ii*) Serve a large enough customer base to provide economies of scale.

(*iii*) Provide continual interaction between packaging developers and users on requirements, design status, schedules, and costs.

(*iv*) Provide off-the-shelf prototype hardware.

(*v*) Provide timely documentation of components, assemblies, specifications, and application guidelines.

(*vi*) Insure that proper computer aids are available for the design of printed wiring boards.

(*vii*) Demonstrate the feasibility of production early in the development cycle.

(*viii*) Plan ahead for manufacturing buildup.

(*ix*) Provide extensions to the hardware family to meet new requirements while maintaining compatibility with existing designs.

The development of *BELLPAC* hardware was mainly the responsibility of the Interconnection Technology Laboratory at Bell Laboratories in Whippany, although invaluable contributions were made by several of the system development organizations. During the development of the hardware building blocks, the objectives listed above were aggressively pursued, and progress was monitored by the committee.

In our view, the development objectives have been successfully met. The number of projects which have chosen to use *BELLPAC* hardware is now large enough to guarantee high-volume manufacturing benefits to even very low-running projects. A broad range of physical design options has been employed in the projects using the *BELLPAC* system, indicating that the trade-offs between flexibility and costs were correct for a majority of the users. Recently, some specialized parts have been added for very high-volume applications. These parts will be available to low-volume users as well, but will have less flexibility in application. The committee which originally served as the steering group for the development of the *BELLPAC* system has now become a part of the *BELLPAC* System Users Forum. Regular meetings are held to review design and manufacturing status.

II. PHYSICAL DESIGN CONCEPTS

The *BELLPAC* hardware family covers a broad range of options in board sizes, pin-out densities, and shelf configurations; these options, however, all stem from a small set of parts and a common design concept. The way in which these parts are designed and assembled is summarized here.

The exploded view of Fig. 1 illustrates the physical design concept. Circuit card connectors contain receptacle contacts. These contacts mate with 25-mil square pins which are press-fit into an epoxy glass backplane. The circuit packs, connectors, and backplanes are described in more detail in later sections. Proper alignment of the circuit card to the pin field is assured by the parts labeled *ramp* and *spacer-aligner* in Fig. 1. The spacer-aligner contains precision-molded apertures that fit over the pins in the backplane and thus align the protrusions on the spacer-aligner. These protrusions serve to align the ramps to the pin field. The ramps, in turn, guide the circuit cards into position.

The support structure for the *BELLPAC* backplane is the mounting plate indicated in Fig. 1. The backplane assembly is self-aligning via precision holes and target pins, so that no special jigging or fixturing is required.

The apparatus housings fasten to the mounting plates and provide support for the circuit cards. Card guides are plastic tracks that snap into the apparatus housing where required. This approach provides minimal blockage of air flow while allowing a modularity of 0.25 in. in circuit card spacing.

As illustrated, a lever for insertion and withdrawal of the circuit cards is incorporated, and a hinged designation strip for identification of circuit card position is provided.

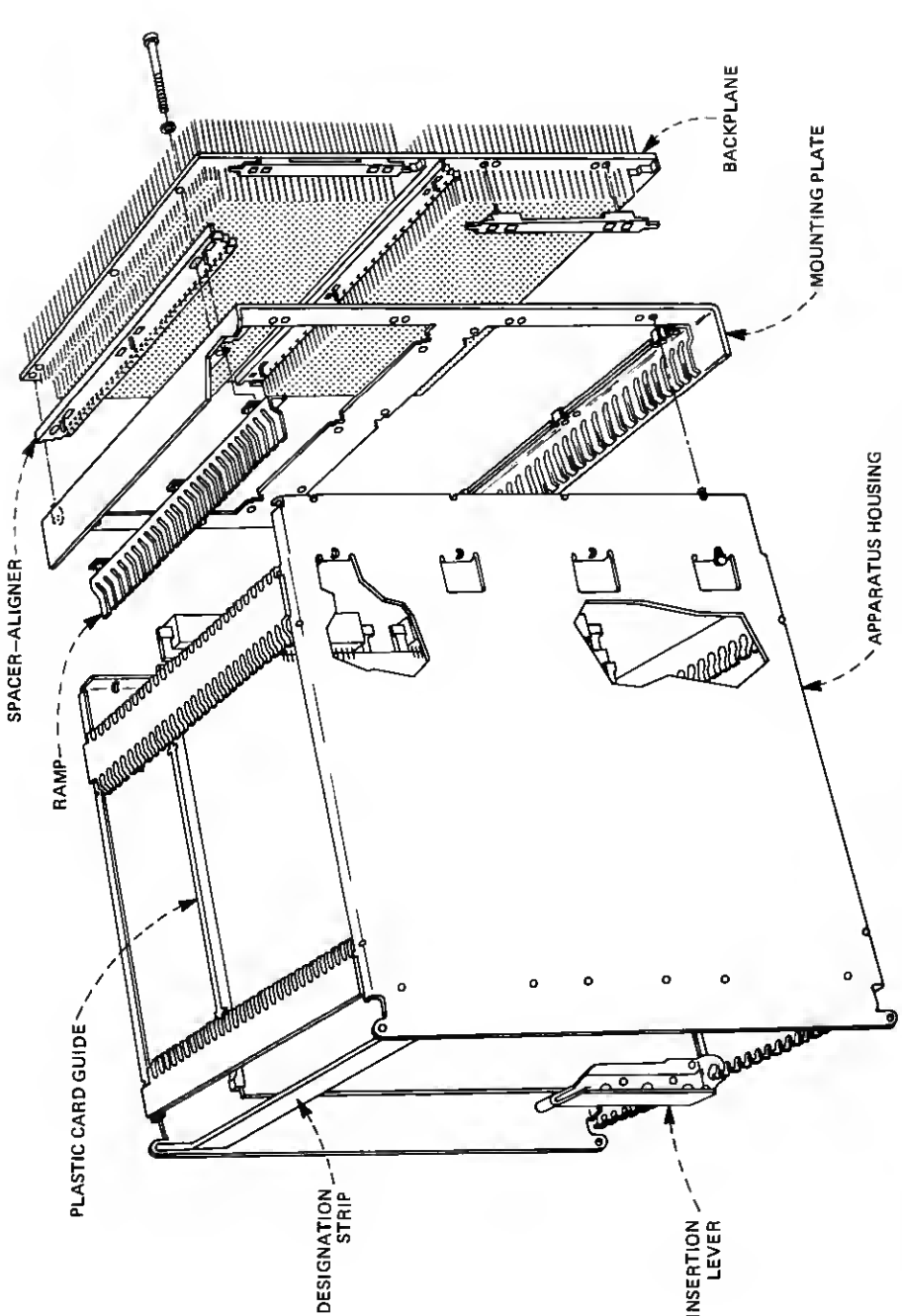
2.1 Compliant pin and circuit pack connectors

A key element of the packaging system is a compliant pin which is press-fit into printed wiring backplanes. The reliability of the compliant pin-to-backplane interface has been established by studies at Bell Laboratories over the past five years. Portions of this work are covered in Ref. 1.

The major experience to date has been accumulated with pins manufactured to Bell Laboratories specification by Winchester Electronics in Oakville, Connecticut. The compliant region, which is of Winchester's design, is in the center section of the pin shown in Fig. 2. (Reference 2 gives further details of the compliant region design.) The large square shoulder section of the pin appears on the circuit pack side of the backplane and is provided as an aid to insertion tool design. Also shown in Fig. 2 is the contact which is the basis for all *BELLPAC* connectors.

A cross-sectional view of the compliant section before insertion is shown in Fig. 3 and after insertion in Fig. 4. The compression of the pin and the intimate contact between the pin and the surrounding plated through hole are clearly shown.

The circuit card connectors that mate with the compliant pins all utilize contacts of the type shown in Fig. 2. The contacts are assembled into plastic housings to provide a family of circuit pack connectors.


BACKPLANE
MOUNTING PLATE
SPACER–ALIGNER
APPARATUS HOUSING
RAMP
PLASTIC CARD GUIDE
DESIGNATION STRIP
INSERTION LEVER

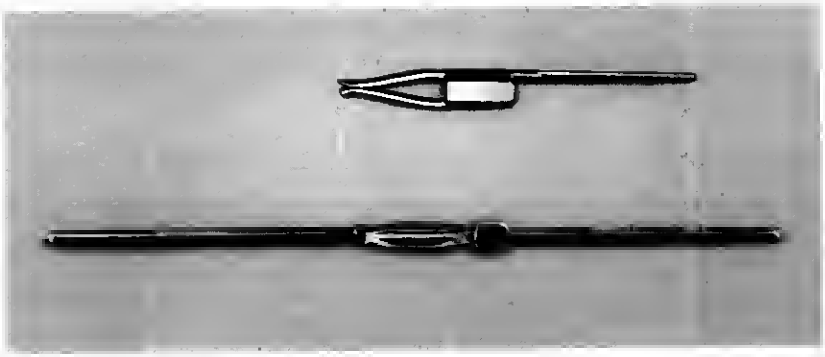


Fig. 2—Compliant pin and connector contact.

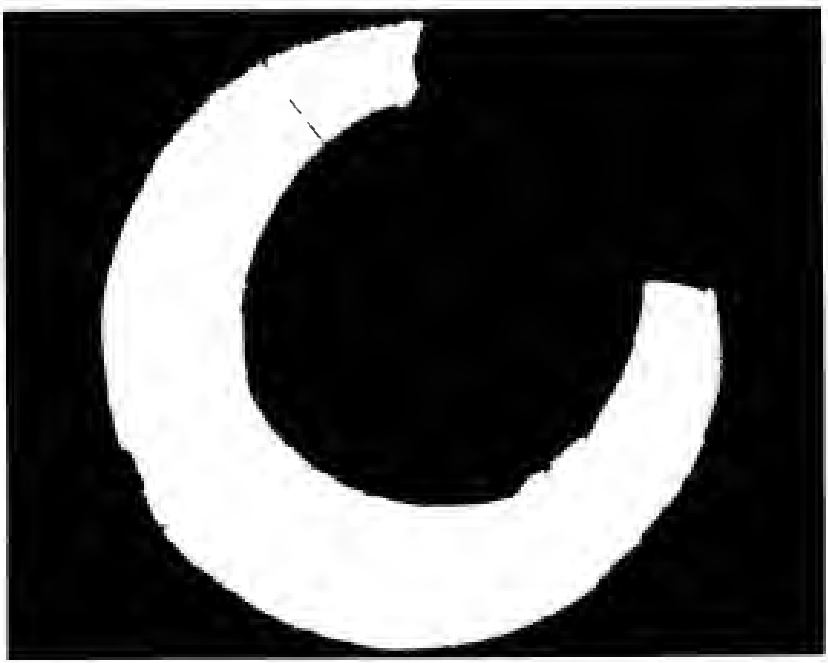


Fig. 3—Compliant pin before insertion.

The connector family is modular in two dimensions. Nominal heights (which correspond to circuit card heights) of 4, 6, and 8 inches are available. The connectors provide variable pinout densities by accessing varying numbers of columns of backplane pins. Connectors are available to mate with 2, 3, 4, and 6 columns of pins. Figure 5 illustrates the *BELLPAC* connector family and indicates the number of contacts available for each code.

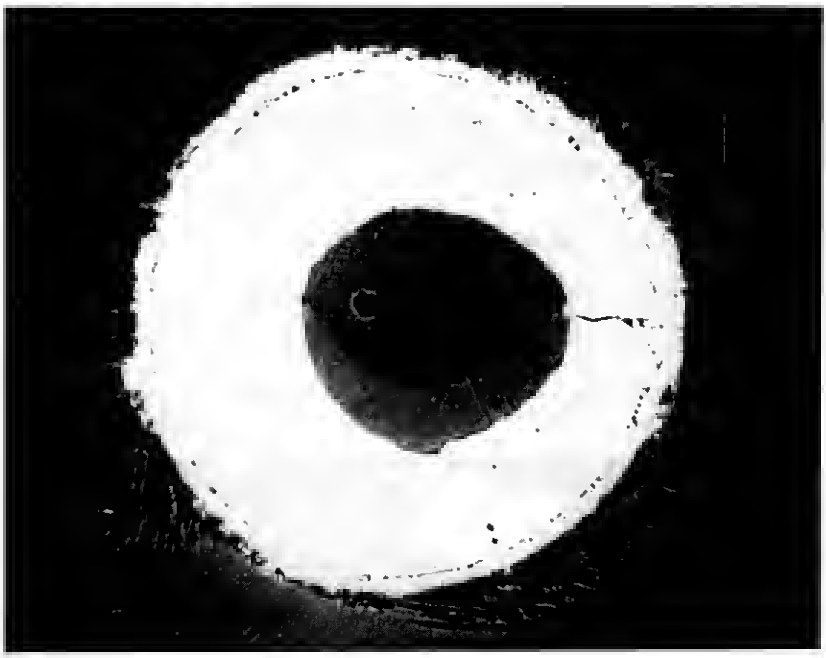


Fig. 4—Compliant pin after insertion.

The lower density connectors with two or three columns of contacts provide 16 or 24 pin-outs per inch of circuit pack height. These connectors are attached to circuit packs by heat-staking plastic posts on the connectors so that they plastically deform and completely fill corresponding holes in the circuit cards. Electrical connections are made by soldering tails of the connector contacts into plated through holes in the circuit cards at the same time as other components are soldered to the circuit packs.

The higher-density connectors with four or six columns of contacts provide 32 or 48 pin-outs per inch of circuit pack height. These connectors are provided with ears so that they may be riveted to the circuit cards. Electrical connections are made in a separate mass soldering operation which reflows the solder on the tails of the connector contacts and their corresponding leads on the circuit packs.

2.2 Compliant pin backplanes

A large degree of design flexibility is inherent in the backplane system. All pins are placed on 0.125-in.-grid positions; however, only those columns of pins required for mating with circuit card connectors or other connectors need be installed. Interconnections among pins in the backplane can be provided by any combination of printed wiring

(double-sided or multilayer), manual wiring, automatic wire-wrap, and backplane cables (switchboard or tape). All pins are designed to allow three wire-wrap levels or two wire-wrap levels and one backplane connector engagement on the wiring side of the backplane. On the circuit pack side, the pins may extend either of two heights above the backplane to allow early make/late break capability.

A backplane arranged to accommodate twenty-seven 8-in. high circuit cards is illustrated in Fig. 6. This backplane is approximately 24 in. wide and contains about 3000 compliant pins. A backplane of the same size with a full complement of pins contains 10,800 pins.

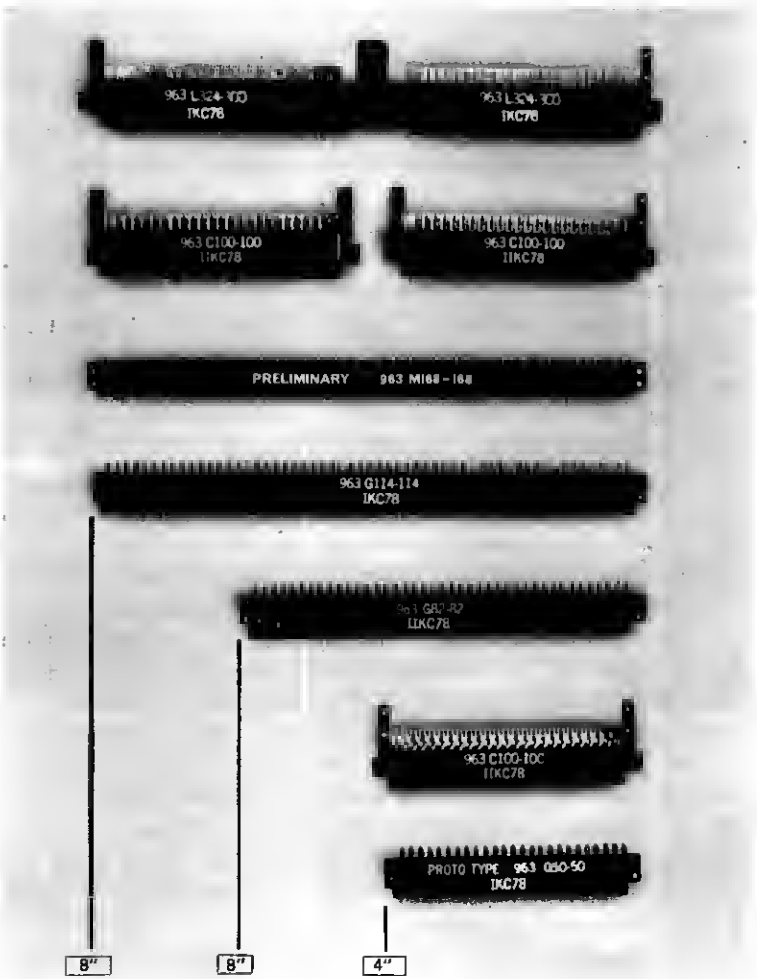


Fig. 5—*BELLPAC* connector family.

Fig. 6—*BELLPAC* backplane.

Typical 8-in. high backplanes designed to date for use in 2-ft., 2-in. central office frames have contained pin counts in the range of 4000 to 8000.

2.3 Circuit packs

Choosing a proper set of circuit pack sizes for inclusion in the *BELLPAC* system was one of the most important phases of its development.

There are eight circuit pack sizes, a sufficient number to satisfy the needs of most projects. There are three circuit pack heights (3.67, 5.67, and 7.67 in.) which fit into apparatus housings of 4-, 6-, and 8-in. heights. Three nominal circuit pack depths are available: 7, 9, and 13 in. The first depth is tailored for use in 12-in. base central office frames with large amounts of backplane wiring and cabling. The 9-in. depth is for 12-in. base frames which have either nominal amounts of backplane cables or cabling accommodated in front-mounted ducts. The 13-in. depth is provided for use in 18-in. base frames with backplane cabling. The chart in Fig. 7 summarizes the circuit pack sizes available and their corresponding connector I/Os (inputs and outputs).

Notice from Fig. 7 that only six circuit pack sizes have been put into use. The 6- by 7-in. and 6- by 13-in. sizes have not yet been required by any projects. The other circuit pack sizes are not equally popular, but all are being used. Judging by requirements to date, the 8-in. high cards will be much more widely used than smaller cards. Most of the smaller cards being used now have been incorporated into systems which also are using 8-in. high cards.

The 8- by 13-in. size is being widely used and seems to support a general trend toward building much more complex plug-in modules than in past systems.

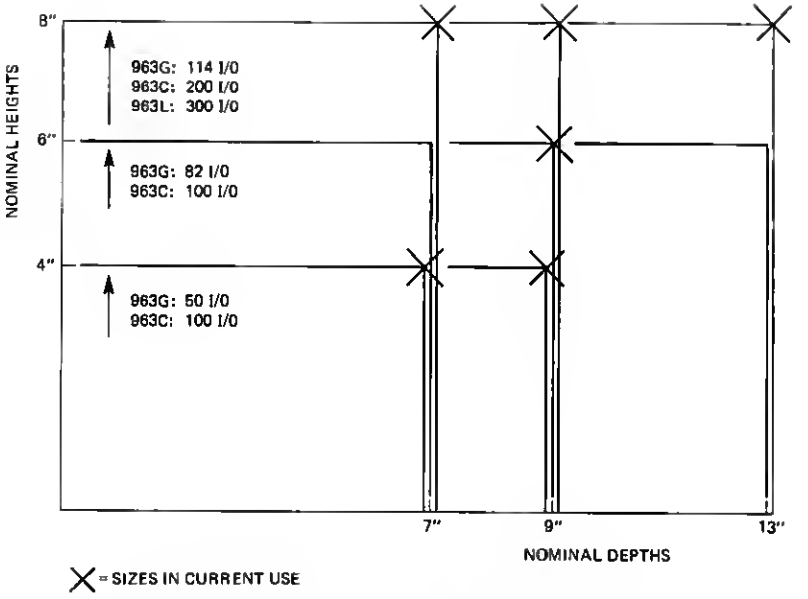


Fig. 7—Circuit pack sizes.

Circuit packs may be fabricated in a variety of technologies. Choice of circuit pack technology is dictated by many factors, including cost, electrical performance, thermal performance, and interconnection density. *BELLPAC* system designs are currently supported in the following circuit pack styles:

(*i*) Double-sided epoxy glass (both conventional and fineline with bus bars).

(*ii*) Double-sided epoxy-coated metal.

(*iii*) 4-layer multilayer board.

(*iv*) 6-layer multilayer board.

(*v*) Wire-wrap.

(*vi*) Quick connect.

The last two board styles are designed for rapid system breadboarding and are available as off-the-shelf parts to be wired by the user.

By way of example, an 8-in. high by 9-in. deep circuit pack is shown in Fig. 8. This double-sided rigid card has a 114-pin connector and low wiring density. By contrast, other cards designed in *BELLPAC* system technology have packaged as many as 150 DIPS (dual in-line packages) on 6-layer, fineline multilayer boards.

2.4 Common features

An extensive set of drawings has been generated to define common features for *BELLPAC* circuit cards. The term "common features"

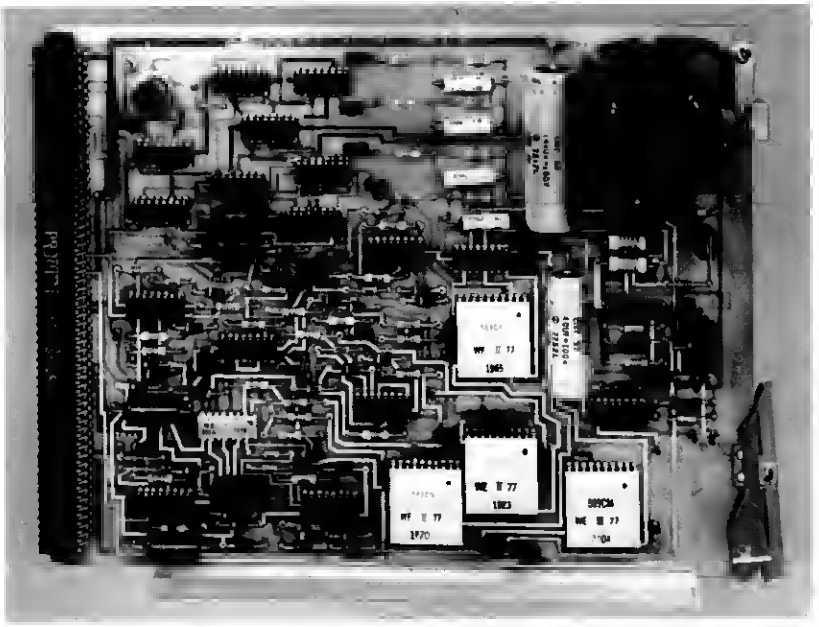


Fig. 8—*BELLPAC* circuit pack example.

refers to the fact that all those circuit pack characteristics common to a particular class or style of *BELLPAC* circuit cards have been identified and defined. There are two types of common features: physical common features and artwork common features. The physical common features define exact board dimensions, tooling holes, void areas for components, connector mounting holes, etc. The artwork common features define connector attachment lands, pattern feature sizes, board layups for multilayer boards, and a very large number of other printed pattern features.

The development and dissemination of common feature information have provided the following advantages:

(*i*) Facilitates standardization and characterization.

(*ii*) Improves routability and manufacturability.

(*iii*) Allows efficient board topology libraries to be built and used.

(*iv*) Reduces design cycles: Less manual input data required. Fewer input errors.

(*v*) Allows control and dissemination of design and manufacturing changes.

III. ELECTRICAL CHARACTERIZATION

The goal of this effort is to provide a complete electrical characterization of the *BELLPAC* components so that the electrical system

designer may concentrate on those detailed questions specific to the particular system.

Studies have been made on the electrical properties of *BELLPAC* connectors, cables, and circuit packs. The transmission properties of the connector family were studied and found to be adequate for the circuit pack needs of almost all present Bell System projects; that is, those with signal rise times of 2 ns or greater or with bandwidths of 175 MHz or less. Another study showed the stability of the electrical connection from the circuit pack to the backplane through the connector. Changes of less than 0.80 milliohm were observed over the lifetime of the connector (200 insertions and withdrawals) with worst-case temporal changes (within 30 seconds of insertion) of less than 0.08 milliohm.

The transmission properties of the connector were found to be dependent upon the grounding pattern used. Similarly, proper attention to grounding patterns is important for the proper use of flat cable. In particular, a study showed that stacks of Western Electric-manufactured PVC flat cable, when properly grounded, have sufficiently low pulse crosstalk to allow the replacement of more expensive coax, shielded wires, or Teflon* flat cable.

Studies of pulse transmission properties (characteristic impedance, propagation delay, rise time, and bandwidth) were made earlier in rather general terms for various circuit pack styles. The development of the *BELLPAC* system, with its specified circuit pack styles and common features, enabled this work to be expanded upon and applied directly to the *BELLPAC* system styles.[3] Detailed evaluation of crosstalk properties, which are strongly geometry-dependent, became possible. Table I is adapted from Ref. 3. (Some material is presented in the table on styles not currently supported in the *BELLPAC* system, namely, the bonded board and the 8-layer multilayer board, or MLB.) The reference presents theoretical results and theoretical scaling laws which extend the application of the crosstalk results to arbitrary pulse signals, periodic signals, and random signals. The material has been used for choice of an appropriate circuit pack style, for crosstalk estimation (either manually or for post-routing analysis, using computer-aided design, or CAD), for estimation of conductor capacitance and inductance, and to estimate the effects of proposed new dielectrics or geometries.

Similarly, an earlier study on current-carrying capacity[4] is being applied and extended to encompass all the *BELLPAC* system styles of printed wiring. Once again, the standardization associated with the *BELLPAC* system makes this detailed analysis feasible.

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Table I—Summary of the pulse transmission properties of various circuit pack styles

Circuit Pack Style	Characteristic Impedance (ohms)	Propagation Delay per Ft. (ns/ft)	Tr (ns)	Band-width (MHz)	Maximum Interlayer Pulse Crosstalk (Near-End) (percent)	Maximum Intralayer Pulse Crosstalk (Near-End) (percent)	For more details, see the following figures in the appendix to Ref. 3
Wire wrap	125 ± 50 160 ± 35	1.4 1.3	2.0 1.8	250 278	—	40 35	4
Extender board	70 ± 5	1.8	1.3	385	0.3	1.6	5
Double-sided (epoxy)	150 ± 20 150 ± 20	1.5 1.5	2.6 2.6	190 190	21 24	39 34	6
Double-sided (metal)	98 ± 8 83 ± 6	1.5 1.5	2.6 2.6	190 190	1.2 3.2	15 13	7
Bonded board	95 ± 10 85 ± 10	1.5 1.5	2.6 2.6	190 190	38 44	21 19	8
4L MLB (EXT P/G)	95 ± 35 85 ± 30	1.8 1.8	2.5 2.5	200 200	20 21	30 16	9
6L MLB (EXT P/G)	75 ± 30 70 ± 35	1.8 1.8	2.5 2.5	200 200	40 46	32 16	10
6L MLB (INT P/G)	68 ± 3 61 ± 3	1.9 1.9	1.8 1.8	278 278	0.5 0.5	20 15	11
6L MLB (INT P/G, surface routing)	85 ± 25 75 ± 15	1.5 (surface), 1.8 1.5 (surface), 1.8	1.8 1.8	278 278	22 26	16 14	12
8L MLB (INT P/G)	85 ± 25 75 ± 15	1.9 1.9	1.8 1.8	278 278	20 24	18 12	13

IV. COSTING AND PARTITIONING COMPUTER AIDS

The computer-aided design specialists at Bell Laboratories are responsible for ensuring that existing and future Bell Laboratories computer aids to design are readily applicable to the *BELLPAC* system. In addition, the specialists are developing one specific, new, stand-alone program, a *BELLPAC* system costing and partitioning analysis program.

The goal is to develop an interactive system that will help the physical designer answer some questions which arise during the design process. A large number of parameters must be considered by the designer, including circuit pack parameters (size, type, spacing, and technology) connector mix, hardware costs, design intervals, power dissipation, electrical bandwidth, and many others. An output from one problem solution may well be the input to another. Some problems are quite straightforward, such as obtaining the cost (prototype or production) and the parts list for a specific shelf assembly. Others are more subtle, such as determining an appropriate division of available frame space into various heights or apparatus housings and circuit packs, with appropriate pin-outs per circuit pack, under various physical, thermal, or electrical constraints. It became apparent that one interactive system could efficiently handle many of these questions. In cases where much is known (such as where a parts list is required), the user will enter the known data. In other cases, theoretical relationships will be necessary to produce some of the needed data.

Much effort has been expended to determine the proper environment for this program. The decision has been made to program in C for a *UNIX** system environment with compatibility to other environments being maintained.

V. ASSEMBLY

Traditionally, the physical designer (e.g., Bell Laboratories) has not specified manufacturing or assembly methods, except as they may be implied by the end-product requirements. The production methods are then left up to the manufacturer (e.g., Western Electric). With design of the *BELLPAC* system, the designer has accepted the responsibility of ensuring the availability of workable, efficient, and cost-effective methods of assembly.

This does not infringe on the traditional prerogatives of the manufacturer, since much of the development of assembly equipment and methods is still performed by Western Electric, specifically at the Engineering Research Center. The designer's function is to disseminate

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this information, to help avoid duplication, and to solve particular problems where the designer has particular expertise. These goals are met through leadership or membership on standing committees, through the maintenance of a prototype assembly shop at Bell Laboratories in Whippany and through special studies in critical areas. We discuss each of these topics briefly.

5.1 Committees

There are two ongoing groups of interest here: As part of the *BELLPAC* Forum, mentioned earlier, approximately every three months a group of Bell Laboratories and Western Electric engineers meets to disseminate and discuss the latest manufacturing and assembly developments, problems, and successes. The second group is the Western *BELLPAC* Manufacturing Task Force. This group has Western Electric Department Chief representation from Interconnection Engineering, from Corporate Engineering, and from locations involved in component manufacture, assembly, and assembly tooling development. In addition, there is a Bell Laboratories representative. The group coordinates the initial and on-going manufacturing process utilizing a corporate perspective. It also oversees development activities to avoid duplications or omissions.

5.2 BELLPAC prototype assembly

A prototype assembly shop and laboratory is in operation at Bell Laboratories in Whippany, and is available for alignment, heat-staking, and soldering of connectors to *BELLPAC* circuit packs. This shop is also capable of assembling apparatus housings and backplanes and inserting compliant pins into backplanes. Measurement facilities for end product inspection are available.

Some equipment available is shown in Fig. 9, including (counterclockwise from upper right) alignment of connectors to the circuit pack, heat-staking of the connector, and the end-product inspection for connector to board squareness and for connector tail protrusion below the board. Equipment is either identical to that used in production or similar enough that experience gained can be transferred. For example, at present, one post is heat-staked at a time, while the production equipment stakes all 14 posts simultaneously. However, the staking cycles (time, temperature, and pressure) are sufficiently similar to enable experience gained in one location to be used in another.

5.3 Specific studies

At first glance, the *BELLPAC* system warp requirements for printed wiring products appear to be more stringent than usual. Actually, since

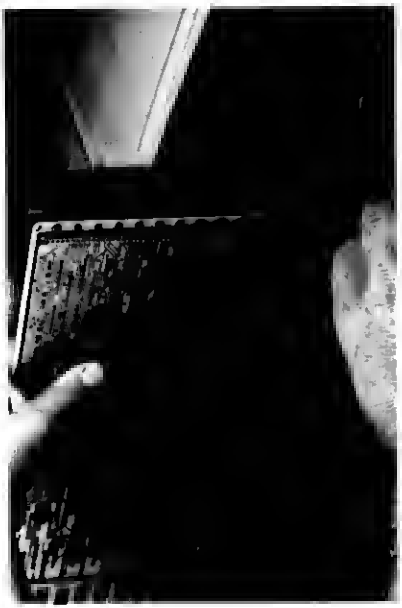

Fig. 6. BELLPAC — A programmable tool.

the requirements are to be measured in a use-related, rather than in a conventional, manner, it is expected they will prove to be a relaxation from the usual (except for printed wiring boards, or PWBs, on 0.5-in. centers). The concept of use-related measurement of warp is illustrated in Fig. 10.

The designers capitalize upon the fact that the *BELLPAC* system physical design is "tight" enough that a considerable amount of board warpage can be tolerated because of the straightening action of the card guides and apparatus housing. Furthermore, the connectors themselves maintain the PWBs straight enough (in the vertical direction) so that, if the board mates properly with the ramp (i.e., in the horizontal direction), it will mate properly with the backplane pins. In addition, detailed studies of proper soldering techniques (e.g., fixturing), of improvements in standard wave-soldering machines and of improved soldering machines have been made. These studies will continue, and others will be initiated as needs arise in the assembly area.

VI. REPAIR

Repair of *BELLPAC* printed wiring boards and assemblies, like any other PWBs or PWB assemblies, is already specified. However, in at least two new areas repair developments are needed, and Bell Laboratories is committed to supplying these needs. These areas are the

Fig. 10—*BELLPAC* system warp measurements.

repair of connectors and the repairs associated with, or required by, the use of compliant pins press-fit into backplanes.

Repair techniques for connectors are available for individual contacts and for individual contacts of connector assemblies. Satisfactory techniques also exist for the removal of connectors from PWB assemblies.

The use of compliant pin backplane assemblies has eliminated the need for soldering and thus further increased printed backplane reliability. (The reliability of the pin-PWB connection has been established in detail.) This has made possible the removal of defective pins and the insertion of replacement pins by simple procedures, employing hand-held tools.

A new repair need has occurred because of the use of compliant pins. When repairing or modifying multilayer printed wiring boards, one may wish to remove the electrical connection of the backplane pin to the backplane plated through hole (PTH). The present techniques assume that the pin is mechanically secured by a connector housing. Since this is not true for the compliant pin used in the *BELLPAC* system, mechanical retention as well as electrical isolation must be provided by the repair method. Two repair techniques have been developed to meet this need. In the first, the PTH is drilled out and replaced by an isolation bushing, and a standard pin is inserted. In the second, an insulated pin is inserted into the PTH in place of the original pin; this version is ideal where the connections in the MLB do not need to be broken, since the potentially dangerous hole-drilling operation is not needed. Isolation bushings and insulated pins are expected to be used for both repairs and modifications.

Welding procedures are also being investigated to avoid soldering when adding modification or repair wiring to compliant pins. These and other repair techniques will continue to be developed as needed.

VII. PROJECT APPLICATIONS

Currently, over 40 projects use *BELLPAC* hardware. Many more are studying its applicability to their needs. *BELLPAC* hardware was first shipped to an operating company in May, 1978. The first system, called AMARC, uses 8- by 13-in. circuit packs—generally as low-density double-sided boards carrying large numbers of relays and other large components. Even though the component density was low, applications required the use of 200 pin connectors on some cards. The AMARC shelf assemblies mount within relay rack housings for compatibility with minicomputer equipment. We mention these details because, in several ways, this application typifies systems which capitalize on the benefits provided by *BELLPAC* hardware. The system was partitioned optimally by choosing appropriate building block sizes from the range

available. Sophisticated interconnection products were readily available, allowing development intervals to be kept short. And low costs were achieved, even though manufacturing volumes were low.

Not all *BELLPAC* system projects are low volume, of course. Two electronic switching projects now in development are being completely packaged with *BELLPAC* hardware and will generate very high manufacturing volumes. These high volume programs and others like them will keep hardware and design costs low for all users.

VIII. SUMMARY

The *BELLPAC* system has become a successful technology for packaging Bell System electronic hardware. It consists of a proven set of components and associated documentation. It has been shown to provide both cost and time savings to system area projects. Its flexibility provides the capability for packaging a variety of different systems in a compatible manner. And, most important, the *BELLPAC* system has the development support from both the systems areas and the component areas to assure that the technology will continue to evolve to meet the packaging needs of the next generation of hardware.

IX. ACKNOWLEDGMENTS

Many people have contributed to the design and implementation of the *BELLPAC* system. The authors particularly wish to acknowledge the efforts of J. G. Brinsfield in formulation of the concept, of H. J. Scagnelli in the successful physical design of the hardware system, and of C. L. Winings in the design and implementation of the connector system.

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